OLLSCOIL NA hÉIREANN
THE NATIONAL UNIVERSITY OF IRELAND

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

SUMMER EXAMINATIONS 2009

BSc Honours

Computer Science
CS4403 Introduction to Embedded Systems

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Dr. Richard Studdert

Answer all questions
(Total 80 Marks)

Time 11/2 Hours

1 (a) The drive capability of the address output of a microprocessor IC is as follows: It can source 400μA at logic high and can sink 2mA at logic low. It is to be connected to ICs whose total load is I_{IH} = +2mA and I_{IL} = -18mA. A buffer IC is available whose DC characteristics (using the usual notation) according to the relevant data sheet are as follows:

I_{IH} = + 20μA, I_{IL} = - 400μA
I_{OL} = + 24mA, I_{OH} = - 2.6mA

Show, using a diagram, how you would connect the buffer IC between the microprocessor and the load. Clearly show on the diagram the source and sink currents at the various pins and state whether the buffer provides sufficient drive capability for the load. *(8 Marks)*

(b)Explain how the circuit in Figure 1 can be used to buffer a bidirectional data line between a microprocessor data pin and an external system. *(4Marks)*

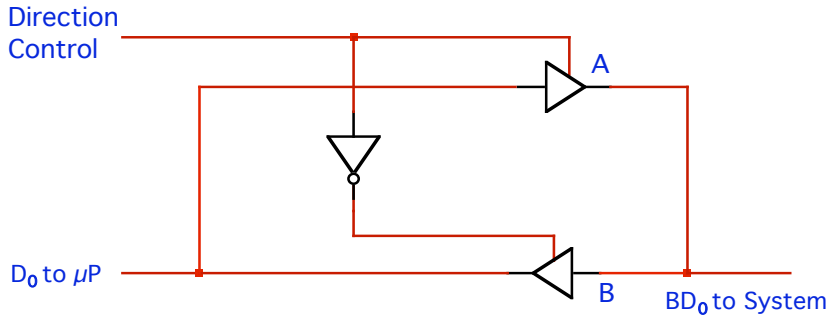

Figure 1

(c) Figure 2 depicts an output system where no actual data transfer takes place. Explain its operation. *(4 Marks)*

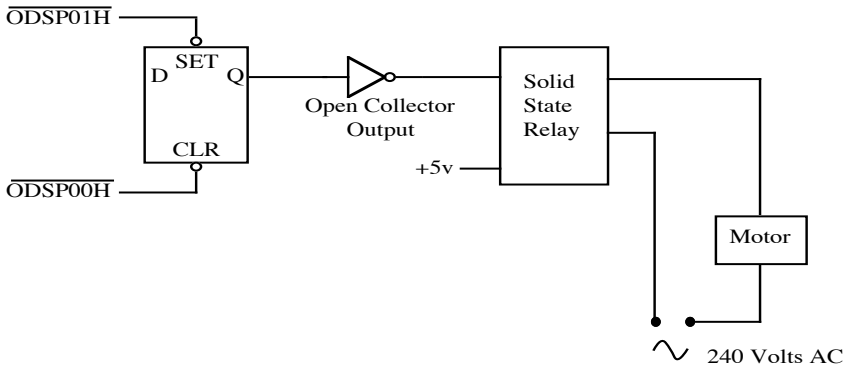

Figure 2

2 Figure 3 shows how eight input devices might be connected to a data bus using addresses 00h through 07h. Note that a ninth input address 08h is used. Explain the operation of this input system. *(16 Marks)*

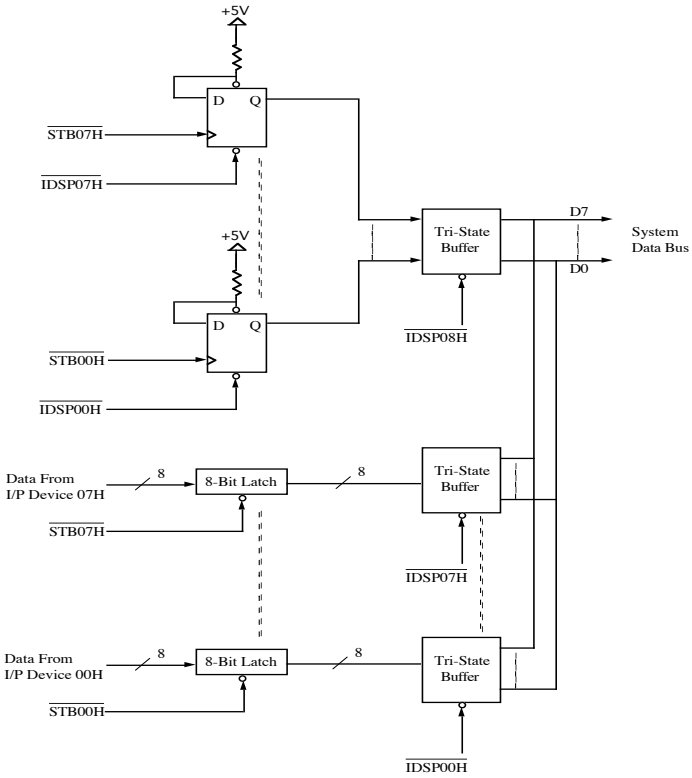

Figure 3

3 (a) Describe the 2-D address organisation used in static MOS IC memory design. Illustrate your answer using a 1Mbit ROM memory IC organised as 128Kx8. In particular, show how the logical word is extracted from the physical word. *(12 Marks)*

(b) What differences in organization would be necessary if the IC in (a) were RW. *(2 Marks)*

(c) What differences from the IC in (b) would be necessary if the RW IC was organized as 1Mbit x 1. *(2 Marks)*

4 Figure 4 shows how up to eight devices can be connected to the vectored interrupt input on the 8085 microprocessor using the Restart instruction. Explain how it works. *(16 Marks)*

The RESTART instruction RST n $0 \le n \le 7$ consists of the following micro-operations:

((SP) - 1) ¬ (PCH) Load contents of PC onto the stack
((SP) - 2) ¬ (PCL)
(SP) ¬ (SP) - 2 Decrement stack pointer
(PC) ¬ 8*n Place the restart address, i.e. 8*n, in the PC

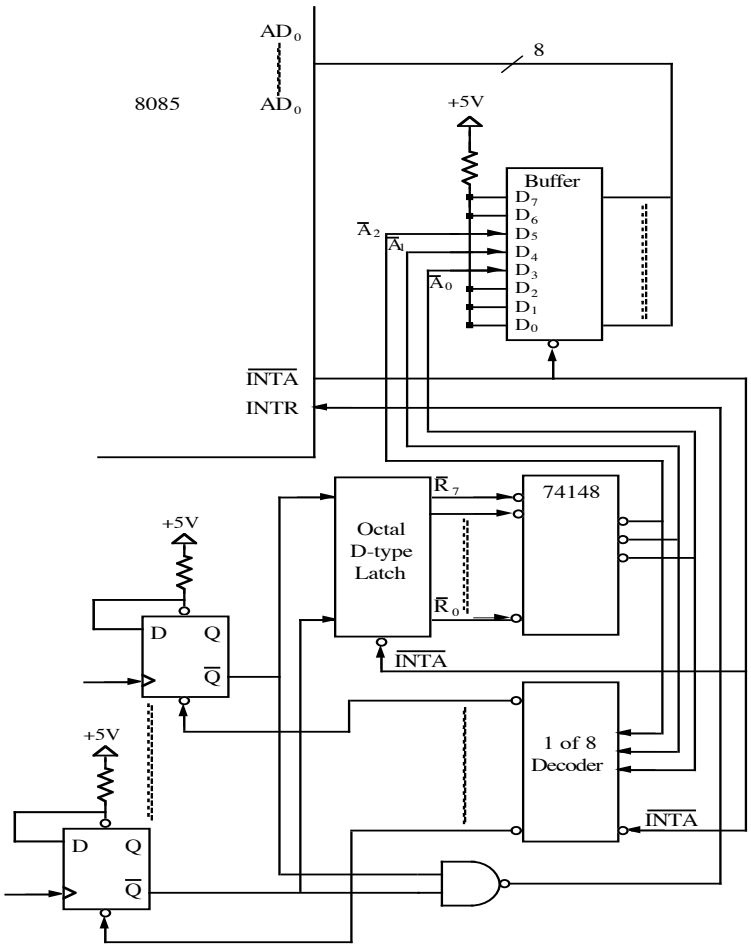

Figure 4

5 (a) In the context of asynchronous serial transmission:

(i) What functions do the start and stop bits perform and what should be their polarities? *(2 Marks)*

(ii) Why should the receiver clock rate be a multiple of the bit rate? *(2 Marks)*

(b) In the context of character oriented synchronous serial transmission:
What levels of synchronisation are used, what is meant by data transparency and how is it accomplished?
(6 Marks)

(c) In the context of bit oriented synchronous serial transmission:
What levels of synchronisation are used, what is meant by data transparency and how is it accomplished?
(6 Marks)